EM Calorimeter Electronics Schedule (as determined at the 3rd BTeV Electronics Workshop on November 2 & 3, 2000)

November 2000	Specifications for the QIE chip
February 2001	Monte Carlo simulations for occupancy and data rate
February 2001	Decide on method to connect the high voltage to the photo multiplier tube bases.
March 2001	Submit requirements document to Computing Division for EM Calorimetry's needs for the Data Combiner Board functionality that is expected to be incorporated into an EM Calorimetry printed circuit board.
May 2001	Evaluate crystals in a test beam
December 2001	Would like to have a prototype QIE chip in hand

Other issues that were discussed but for which schedules have not yet been developed:
Front end mock-up
Decide on HV distribution
Decide on low voltage / high current power supplies
Determine amount of real estate required for electronics

Session 2C
A discussion took place between Yuichi Kubota, Sheldon Stone, Tim Brennan, Bill Haynes, Marc Larwill, Bob DeMaat

Items discussed:
Test beam
Planned for March of 2001 in Protvino. The main thrust of this test beam effort will be to evaluate the crystals from Russia and China. None of the new electronics will be tested here.

PMT bases
Tim Brennan has been working on a PMT base design.
Does a PMT base for the PMT that Sheldon and Yuichi are interested in already exist at Fermilab? This should be looked in to.

The method of wiring the high voltage to the bases needs to be determined.

Photomultiplier tubes
A tube from Hamamatsu is the current leading candidate.

Custom QIE chip
KTeV has a factor of 2 more light in their crystals than BTeV will have.

Temperature at which to operate the crystals
Running the crystals at 0 degrees C will be advantageous in terms of gain and in terms of the effects of radiation recovery. (From 70 degrees F down to 32 degrees F, the gain increases by 1 percent per degree F.) Try to specify better than 0.5 degree C stability for the operating environment of the crystals. The plan for the testbeam effort is to cycle the temperature down to 0 degrees C.

Single event upsets
The potential amount of impact on the electronics should be evaluated.

Location of electronics
We will need to establish the position of the electronics and the cable lengths prior to the baseline review.

Simulations
There is a need to determine in what way to map the QIE/FEB to DCB to even out the data flow. This is occupancy and data rate dependent. We may have these numbers but they should be re-done. A physicist will be assigned to do a Monte Carlo simulation to answer these questions.

Session 5C
A discussion on **PMT bases** took place between Yuichi Kubota, Sheldon Stone, Sten Hansen, Marc Larwill and Bob DeMaat.
Consider using negative high voltage rather than positive high voltage. A test should be conducted on the PMT at negative high voltage.
Consider bulk supplies for each of the higher current, “lower” voltage stages.
Use resister dividers for the lower current, higher voltage stages.
Consider including about 20 volts of adjustment for one of the stages of each of the PMT’s to implement gain adjustment.

Consider whether or not installing a magnetic shield around each PMT is necessary.

10 MeV is the smallest energy deposit that we need to be concerned with. Photons above 1 GeV are of interest.

Expect the **PMT** to have 5 or 6 stages.
The peak signal should be 100 GeV @ 10 photo-electrons per MeV
The pulse shape will have most of the signal in the first 10 to 20 nS with 99% of the signal in the first 100 nS.

The worst case DC standing current should be 200 micro-amps.

A discussion on **QIE chips** took place between Yuichi Kubota, Sheldon Stone, Charlie Nelson, Marc Larwill and Bob DeMaat.
A combination of the features of the CDF and the MINOS chips would be appropriate.

The CDF QIE has an input capacitance of 2.5 pF for a full scale range of 1300 pC. The KTeV QIE has an input capacitance of 1.0 pF for a full scale range of 500 pC.

We would like characteristics similar to the MINOS QIE but BTeV needs the ability to operate with a clock period of 132 nS rather than 18.9 nS which MINOS is using.

The MINOS QIE has an adjustable input impedance that is optimized for 50 ohms.

CDF uses a 10-bit ADC with their QIE. KTeV uses an 8-bit ADC with their QIE.
MINOS uses an 8-bit ADC with their QIE.

A BTeV QIE could be similar to the CDF QIE6 with the following changes:
Input capacitance of 1.0 pF rather than 2.5 pF.
Input impedance of 50 ohms with an input stage similar to MINOS.

A discussion of **DAQ needs** took place between Yuichi Kubota, Mark Bowden, Margaret Votava, Harry Cheung, Marc Larwill and Bob DeMaat.

Mark Bowden recommended that we consider designing two QIE boards. One for high occupancy needs utilizing two or three optical links and one for low occupancy utilizing a single optical link for sending data off of the board.